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RCE 10/2800

PTO/SB/30 (10/2001)

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**REQUEST
FOR
CONTINUED EXAMINATION (RCE)
TRANSMITTAL**

Address to:
Commissioner for Patents
Box RCE
Washington, DC 20231

<i>Application Number</i>	10/006,334
<i>Filing Date</i>	December 3, 2001
<i>First Named Inventor</i>	KAMESH V. GADEPALLY
<i>Art Unit</i>	2818 <i>#10 RCE</i>
<i>Examiner Name</i>	QUOC DINH HOANG <i>Q. D. Hoang</i>
<i>Attorney Docket Number</i>	NSC1-G0610 [P04402 P01] <i>4/10/01</i>

This is a Request for Continued Examination (RCE) under 37 CFR 1.114 of the above-identified application. Request for Continued Examination (RCE) practice under 37 CFR 1.114 does not apply to any utility or plant application filed prior to June 8, 2001.

1. **Submission required under 37 CFR §1.114**

- Previously submitted
 - Consider the amendment(s)/reply under 37 CFR §1.116 previously filed on _____ (Any unentered amendment(s) referred to above will be entered).
 - Consider the arguments in the Appeal Brief or Reply Brief previously filed on _____
 - Other _____
- Enclosed
 - Amendment/Reply
 - Affidavit(s)/Declaration(s)
 - Information Disclosure Statement (IDS)
 - Other _____

2. **Miscellaneous**

- Suspension of action on the above-identified application is requested under 37 CFR §1.103(c) for a period of _____ months (Period of suspension shall not exceed 3 months; Fee under 37 CFR §1.17(l) required)
- Other _____

3. **Fees** The RCE fee under 37 CFR §1.17(e) is required by 37 CFR §1.114 when the RCE is filed.

- The Director is hereby authorized to charge the following fees, or credit any overpayments, to Deposit Account No. 50-1697
 - RCE fee required under 37 CFR §1.17(e)
 - Extension of time fee (37 CFR §§1.136 and 1.17)
 - Other _____
- Check in the amount of \$ 750.00 enclosed
- Payment by credit card (Form PTO-2038 enclosed)

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED

Name (Print / Type)	ALFRED A. EQUITZ	Registration No. (Attorney / Agent)	30,922
Signature	<i>Alfred A. Equitz</i>	Date	April 3, 2003

CERTIFICATE OF MAILING OR TRANSMISSION

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner For Patents, Box RCE, Washington, DC 20231, or facsimile transmitted to the U.S. Patent and Trademark

Name (Print / Type)	Marsha A. Townsend
Signature	<i>Marsha A. Townsend</i>
Date	April 3, 2003

Burden Hour Statement: This form is estimated to take 0.2 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND Fees and Completed Forms to the following address: Assistant Commissioner for Patents, Box RCE, Washington, DC 20231.



PATENT

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of
KAMESH V. GADEPALLY
Application No. 10/006,334
Filed: December 3, 2001

**For: METHOD FOR MANUFACTURING
AN INTEGRATED CIRCUIT
STRUCTURE WITH LIMITED
SOURCE SALICIDATION**

Box RCE
Commissioner for Patents
Washington, DC 20231

Sir:

This is in response to the final Office Action mailed on February 5, 2003, in the referenced application and is being filed with a Request for Continued Examination of the application. Please amend the application and consider the following remarks.

IN THE SPECIFICATION:

Amend lines 10-13 on page 7 to read as follows (the attached appendix sets forth the amended section of the specification with markings showing the differences between the original text and the text as hereby amended):

accordance with the present invention have been performed. Silicon gates 120 and 122 (typical thickness being in the range between 1500 and 4000 angstroms) overlie the gate oxide layer 110 of MOS transistor structures 104 and 106, respectively. Silicon gates 120 and 122 can be made from either

Group Art Unit: 2818

Examiner: QUOC DINH

**RESPONSE TO FINAL
OFFICE ACTION**

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San Francisco, CA 94104
(415) 433-2250

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, Washington, DC 20231, on April 3, 2003.

GIRARD & EQUITZ LLP

By: Marsha A. Townsend
Marsha Ann Townsend